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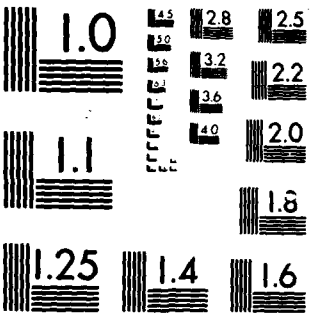

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

(2)

AD-A163 978

BMD PROBE

ON-BOARD PROCESSING

AUGUST 2, 1983

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PROBE PARAMETERS

	1985	1990
SENSOR		
ELEVATION VIEW	15 DEG	22 DEG
SCAN RATE	14 DEG/SEC	36 DEG/SEC
FRAME TIME	5 SEC	2 SEC
DETECTOR VIEW	.1 X .3 MR	.05 X .15 MR
OUTPUT CHANNELS	5250	80000
THREAT		
CREDIBLE OBJECTS	17000	50000
ATTACK CLUSTER OBJECTS	5000	10000
MAX. CLOSE SPACED OBJS.	1500	3000

STARS

20/SQ DEG- LOW BAND
5/SQ DEG- MID BAND
2/SQ DEG- HIGH BAND

GALAXY PEAK DENSITY MULTIPLIER- 5

Accesion For
NTIS CRA&I ☑
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Unannounced ☐
Justification
By
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A-1

LWIR MISSILE SURVEILLANCE SENSOR

- OPTICS

APERTURE	10 IN
SCAN	7 DEG X 7 DEG/SEC

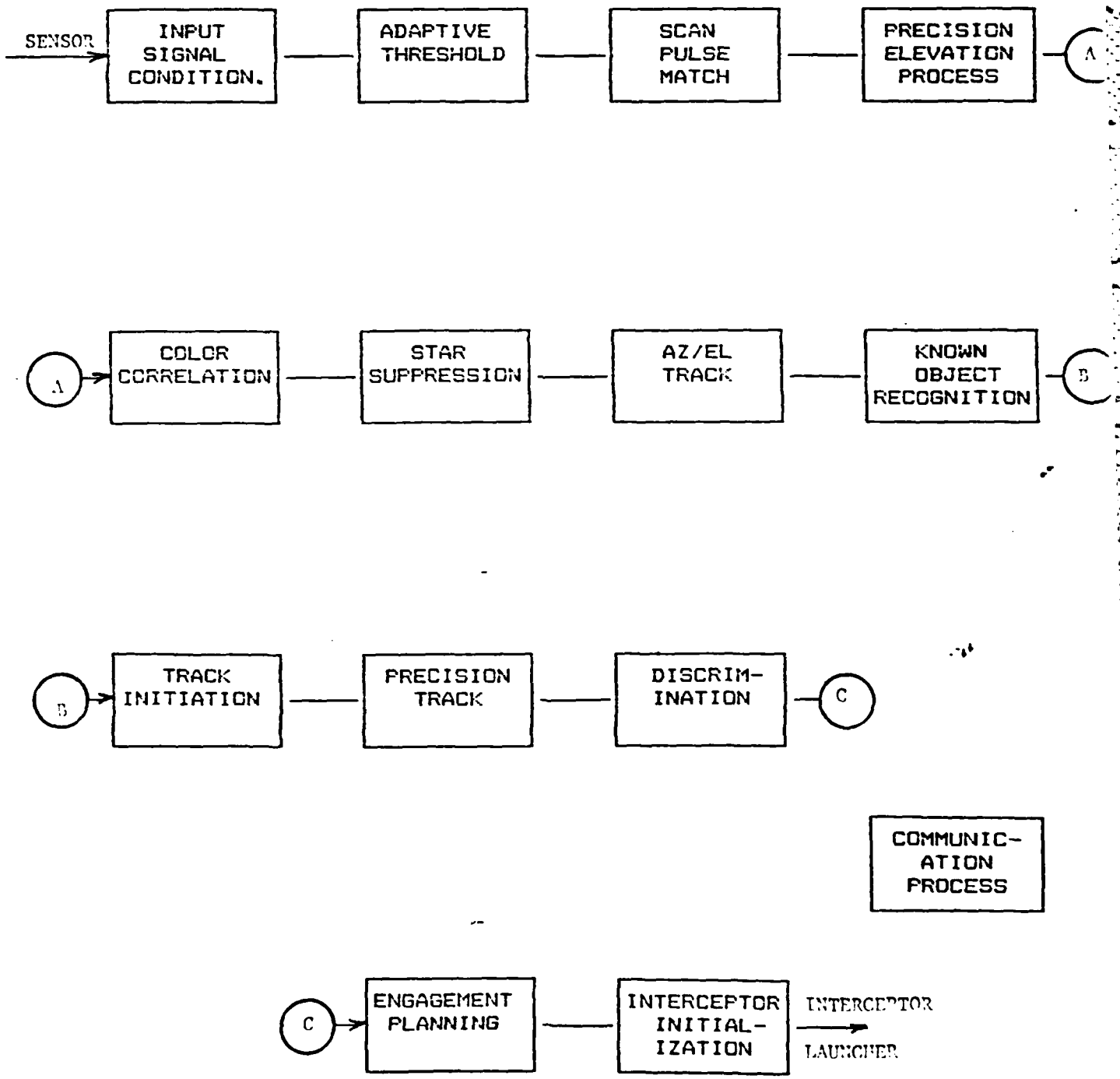
- FOCAL PLANE ARRAY

DETECTORS	1570/COLOR
COLORS	3

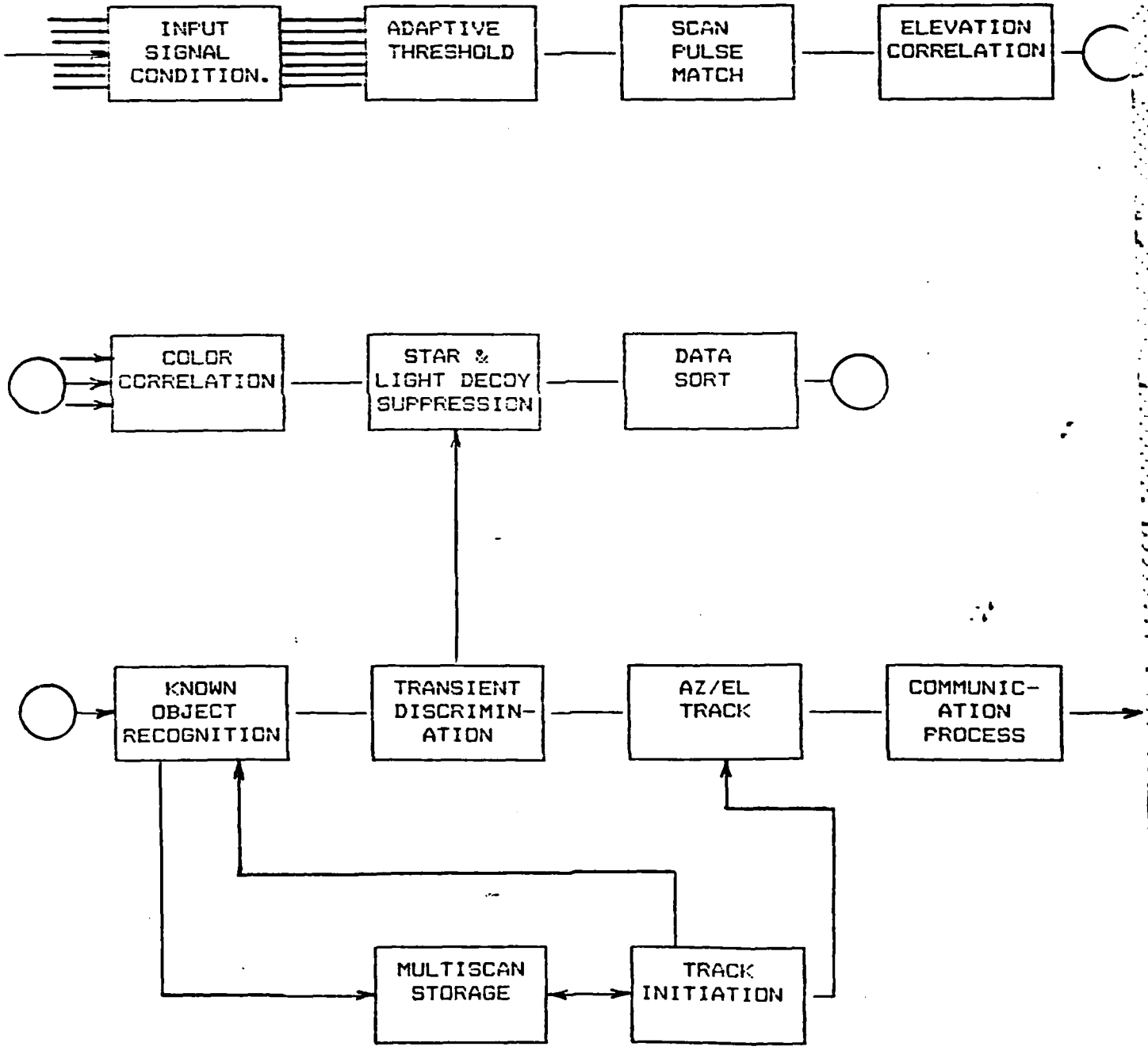
- SAMPLING

DWELL	.8 MS
SAMPLES/DWELL	8
PRECISION	10^{-5} RAD

Missile Surveillance Probe Func. Flow



Missile Surveillance Probe Data Flow



DATA FLOW RATES

FUNCTION OUTPUT	DATA FLOW RATE (FRAME AVE., 1/SEC)	
	1985	1990
A/D CONVERSION	100M SAMPLES	7700M SAMPLES
INPUT CONDITIONING	610K SAMPLES	15.7M SAMPLES
PULSE MATCHING	50K DATA SETS	1.3M DATA SETS
INTRAFRAME CORRELATION	8.5K DATA SETS	43K DATA SETS
TRACK & DISCRIMINATION	3.4K DATA SETS	25K DATA SETS

PROCESSOR ELEMENT

- 20M HZ CYCLE; SIMULTANEOUS 10M HZ INPUT & OUTPUT
- SIMULTANEOUS EXECUTION

  INSTRUCTION FETCH
  ARITHMETIC (EXCEPT DIVIDE)
  SHIFT
  LOGICAL
  COUNT
  BRANCH
  DATA STORE
  DATA FETCH
  INPUT/OUTPUT

- 32 BIT INSTRUCTION
- 64 WORD PROGRAM STORE
- 64 WORD DATA STORE
- 16 WORD STACK
- SINGLE 2 MICRON LITHOGRAPHY CHIP; 4 W

1985 HARDWARE CHARACTERISTICS

	CAPABILITY	BOARD AREA (PERCENT)	AVERAGE POWER (W)
PROCESSOR	10 MAPS	15	2
FAST MEMORY	8K BYTES	2.2	.4
MAIN MEMORY	16K BYTES	2	.1

1985 ONBOARD PROCESSOR

PERFORMANCE

THROUGHPUT-	5130 MAPS
FAST STORES-	13M BYTES
BULK MEMORY-	6M BYTES

PHYSICAL

VOLUME-	2.2 CU FT
HARDWARE MASS-	90 LBS
POWER-	1700 W
BATTERY MASS-	42 LBS

1990 HARDWARE CHARACTERISTICS

AMBIENT ELECTRONICS

	CAPABILITY	BOARD AREA (PERCENT)	AVERAGE POWER (W)
PROCESSOR	20 MAPS	10	1
FAST MEMORY	32K BYTES	2.2	.13
MAIN MEMORY	64K BYTES	2	.05

JOSEPHSON ELECTRONICS

	CAPABILITY	CHIP SIZE	AVERAGE POWER
PROCESSOR	1000 MAPS	1 CHIP	20 MW
PROGRAM STORE	.4 NS ACCESS	860 WDS	20 MW
CACHE MEMORY	.4 NS ACCESS	1000 WDS	16 MW
MAIN MEMORY	7 NS ACCESS	4000 WDS	.32 MW

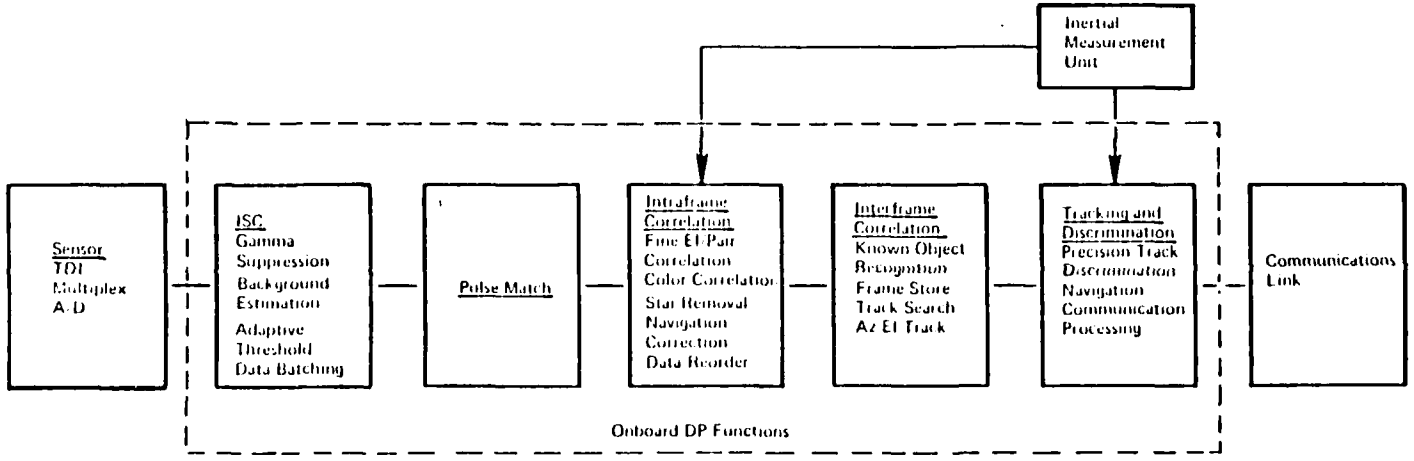
1990 ONBOARD PROCESSOR

PERFORMANCE

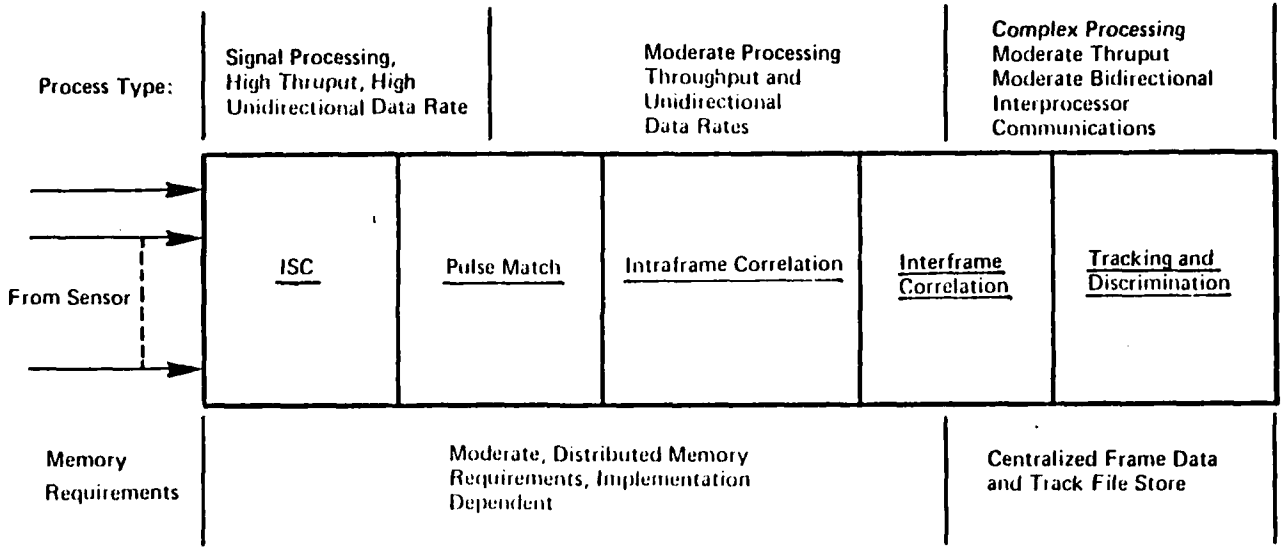
THROUGHPUT-	416000	MAPS
FAST STORES-	15M	BYTES
BULK MEMORY-	27M	BYTES

PHYSICAL

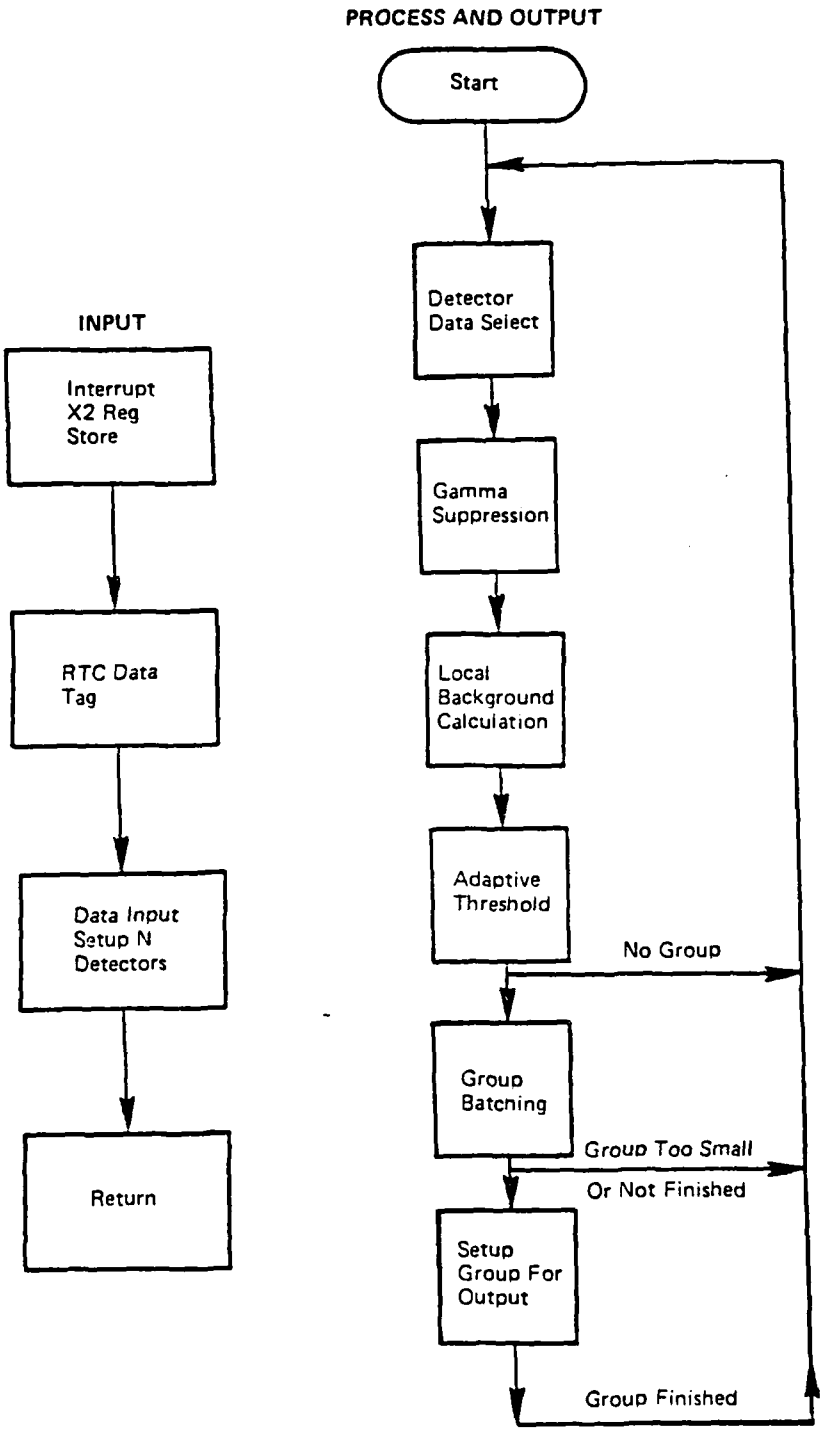
DEWAR VOLUME-	1.3	CU FT
AMBIENT VOLUME-	.4	CU FT
HARDWARE MASS-	57	LBS
POWER-	137	W
BATTERY MASS-	7	LBS



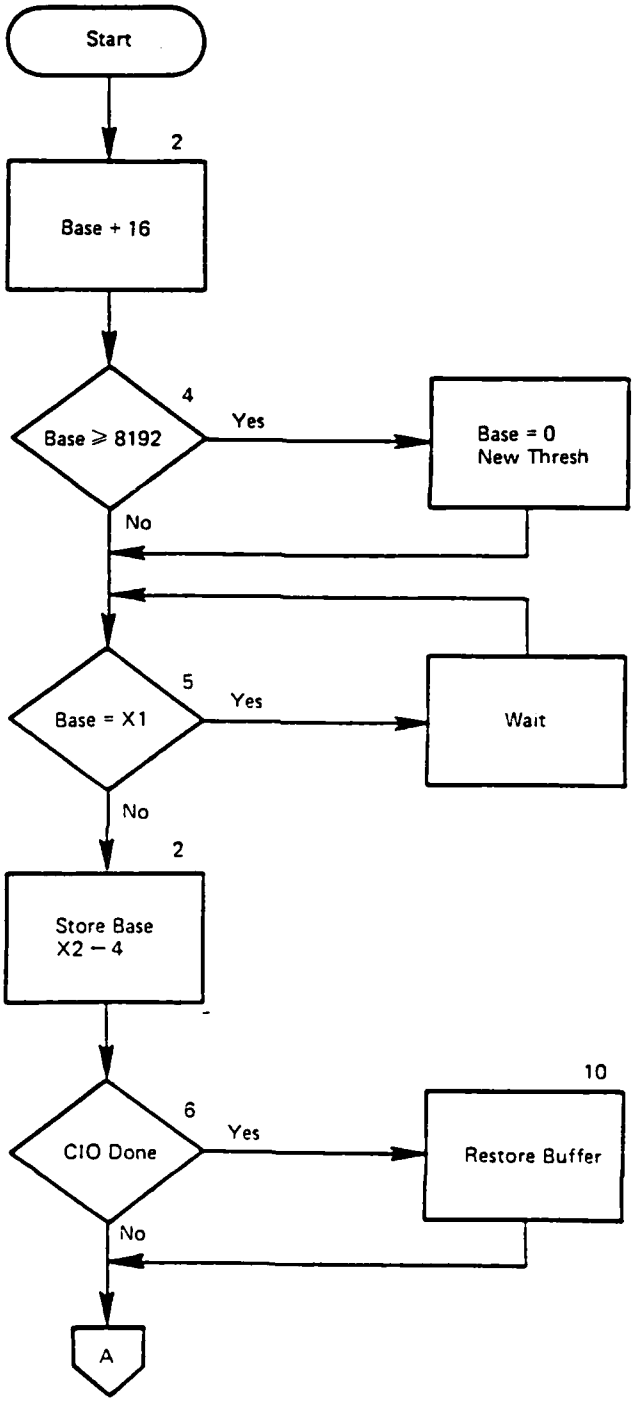
Onboard DP Data Flow Block Diagram



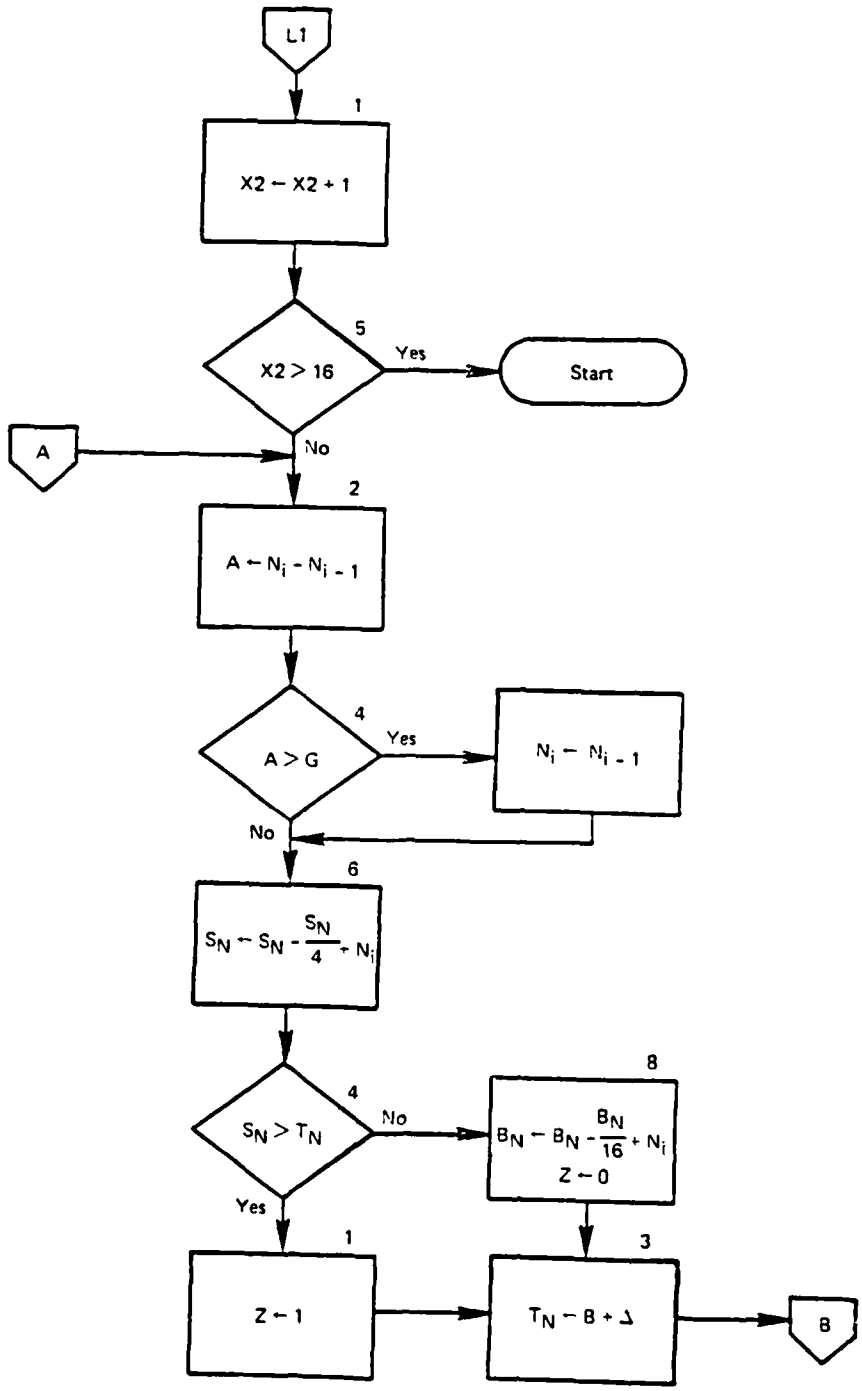
System Partitioning by Processor and Memory Types



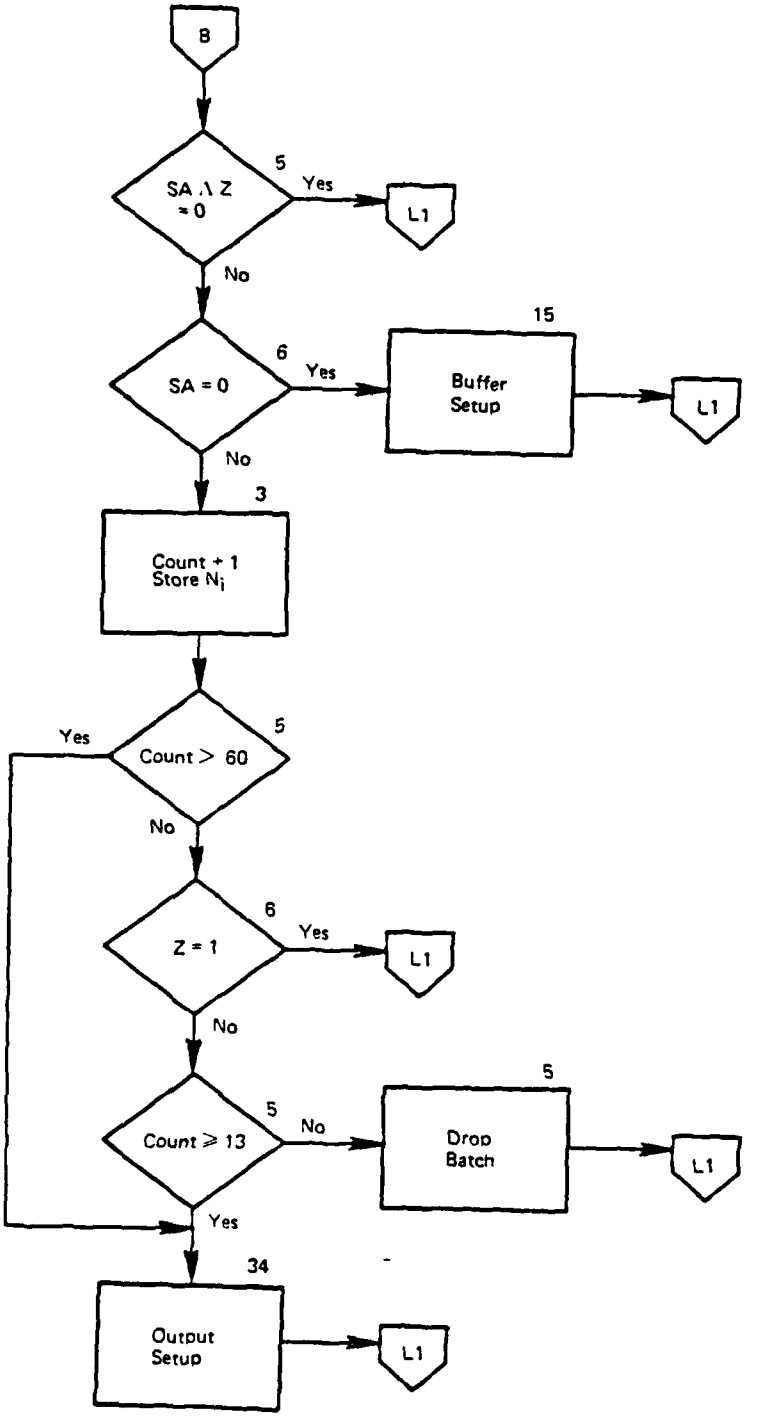
ISC Processing Flow



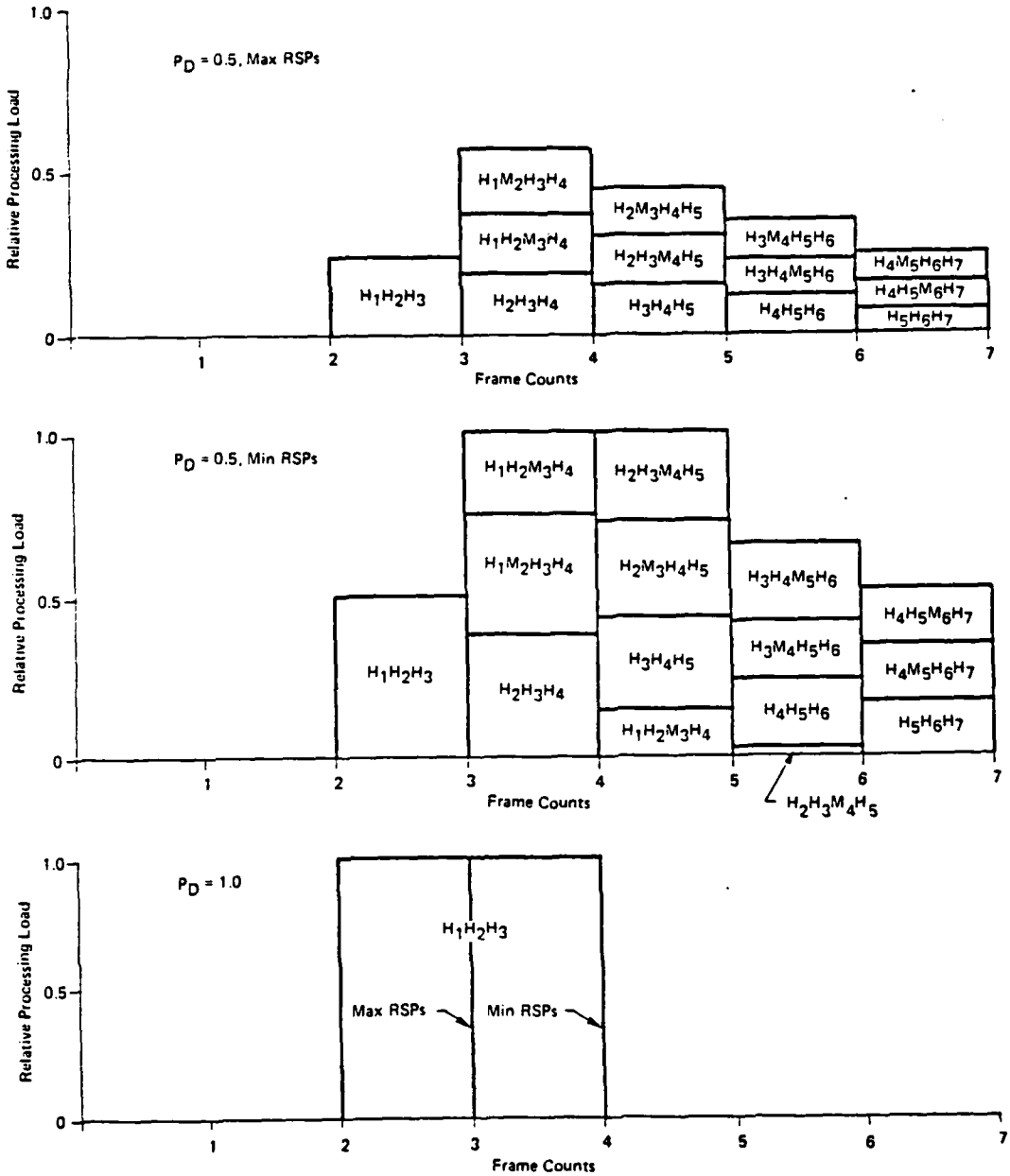
ISC Detailed Flow (Sheet 1 of 3)



ISC Detailed Flow (Sheet 2 of 3)



ISC Detailed Flow (Sheet 3 of 3)



*H means frame data on an object, M means no frame data on an object, Subscript is frame number.

Track Search Load Dependencies

Az-El Track Operations and Data Access Characteristics

Operation	Maximum Access Rates (10 Sec Maximum Duration) (sec^{-1})	Words Transferred Per Access	Processor Cycles Per Access
Receive Track Search data and assign Track Number	3600	9	65
Send Az, El data to KOR	3600	4	10
Receive Az, El correlations from KOR	7200	5	50
Remove Az El data from Frame Store for validated tracks	3600	12	50
Collect amplitudes for Track Initialization		24	50
Precision Track and Discrimination Initialization	7200	24	
Send update data to Precision Track and Discrimination	7200	6	10

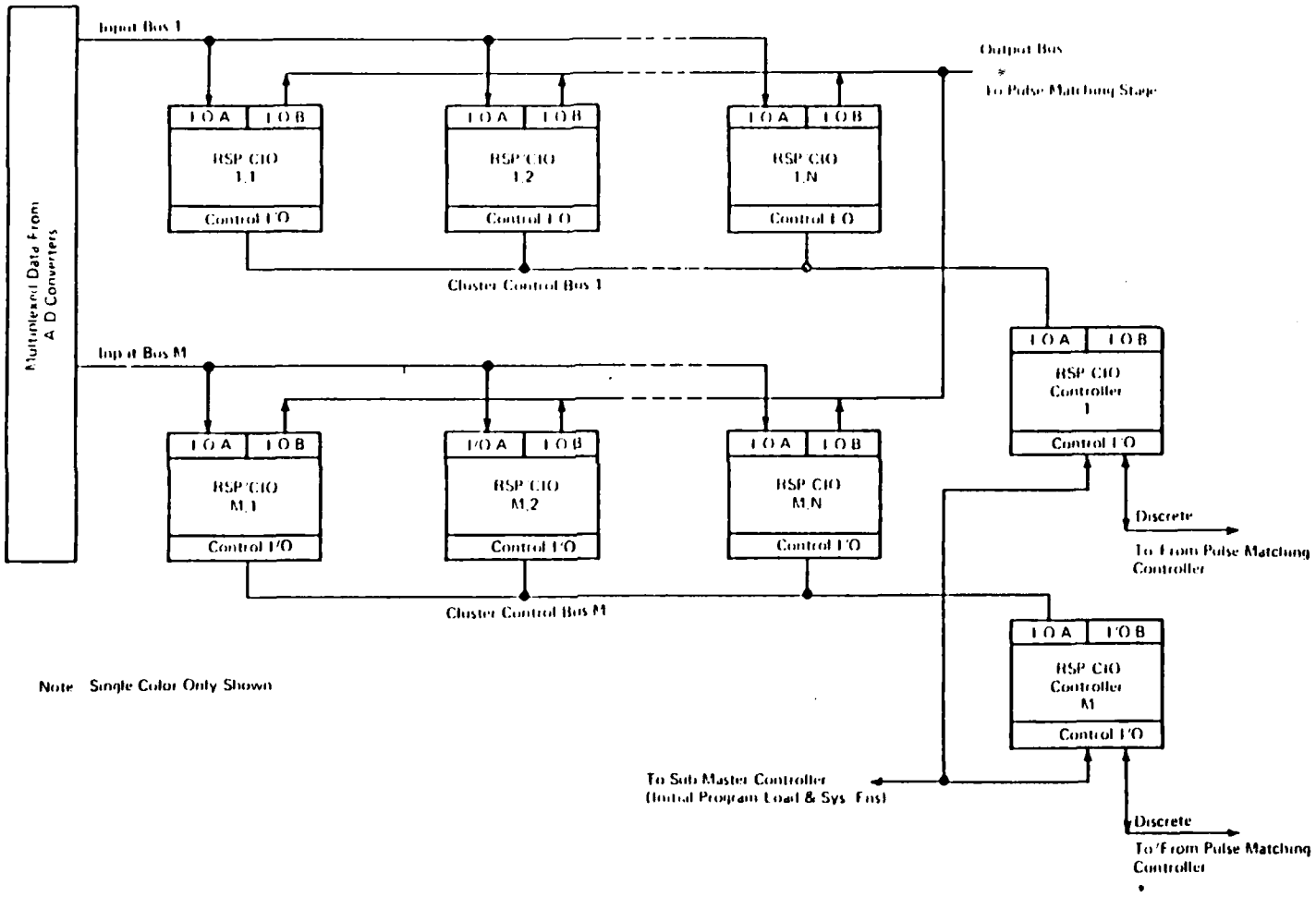
*Note that accesses are not all concurrent.

ISC Process Instruction Count Data

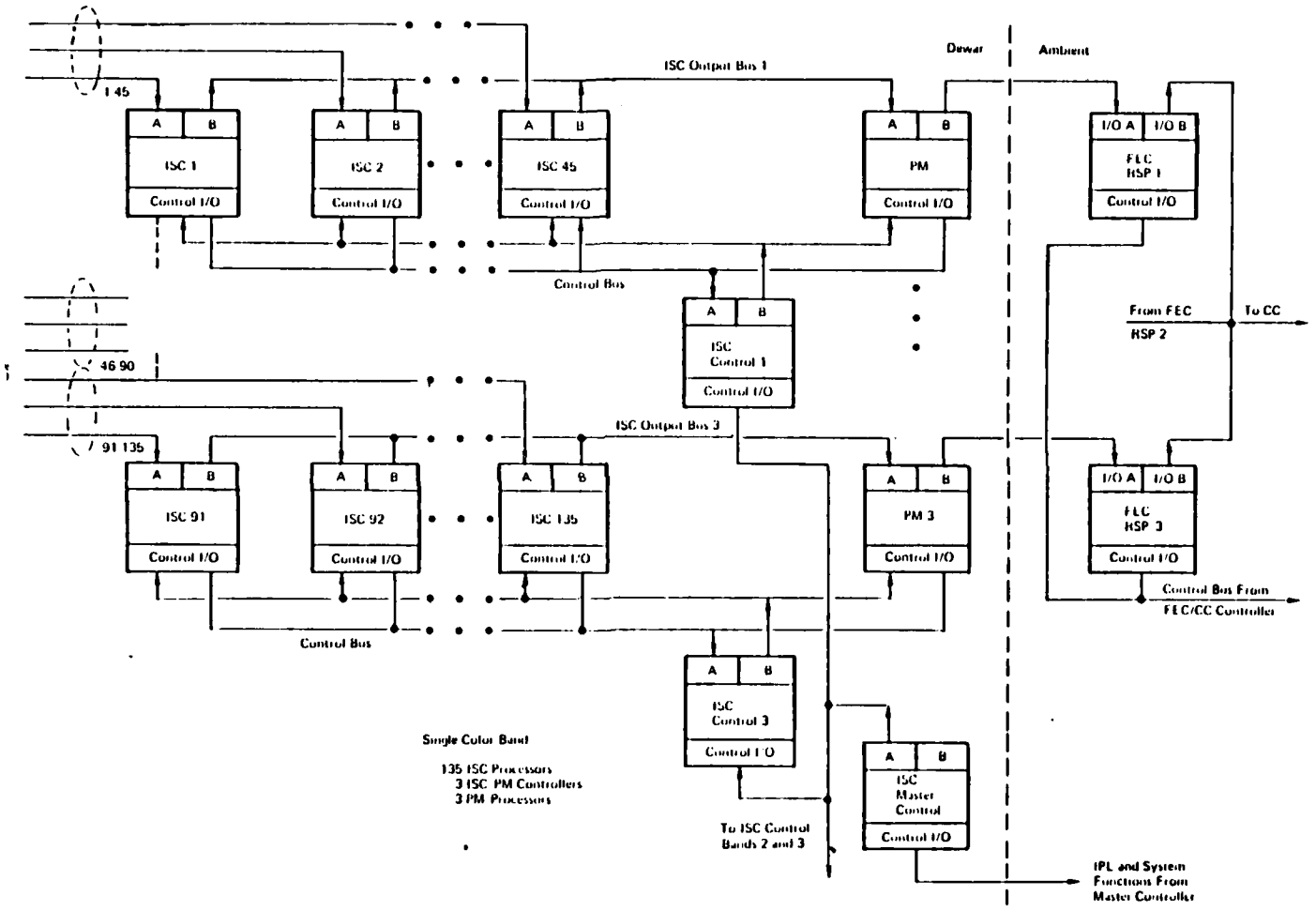
Process Path	Conditions	Instruction Cycles per Data Sample
L1[1]	No signal; no output buffer assigned	36
L2	First detected signal; assign output buffer, store data, correct background	78
L3	Next detected signal sample	58
L4	Next signal sample missed	55
L5	One sample missed and less than 12 in batch	65
L6	Two samples missed and 12 or more in batch	73
L7	60 samples in batch	63
Input Data	All Paths	1
Input Data Setup	All Paths	15/N[3]
Inner Loop Setup	All Paths	19/N[3]
Output Data	Batch size dependent, not L1	24 — 64
Output Busy Clear	Once per output loop set-up	20

(1) 99.3 percent of the samples use this path on frame average and 96.8 percent use it in an attack cluster.

(3) N is number of detectors assigned to an RSP.



ISC Processing Stage Architecture



A. ISC and Pulse Match

1990 Hardware Configuration for JSP Multifunction Implementation (Sheet 1 of 3)

1985 Hardware Sizing Summary

Function	Processor Count (RSPs)	Memory Per Processor[2]	Circuit Board Count	Average Power (W)
Input Signal	438	4K IS, 8K DS	94.6	1402
Conditioning	21[1]	4K IS, 4K DS	3.6	59
Pulse Match	30	4K IS, 8K DS	6.5	96
	1[1]	4K IS, 4K DS	.2	3
Intraframe Correlation				
FEC	3	4K IS, 64K DS	1.6	26
CC	1	4K IS, 128K DS	.9	15
SR/NC	1	4K IS, 8K DS	.2	3
DR	1	4K IS, 64K DS	.5	9
	1[1]	4K IS, 4K DS	.2	3
			3.4	56
Interframe Correlation				
KOR	1	4K IS, 100K DS	.7	12
FS	1	4K IS, 4K DS, 256K BM	.8	5
TS	5	4K IS, 16K DS	1.3	20
AET	1	4K IS, 4K DS, 576K BM	1.6	7
	1[1]	4K IS, 4K DS	.2	3
			4.6	47
Track and Discrimination				
PT/D	4	12K IS, 4K DS, 512K BM	6.1	28
CP	1	4K IS, 16K DS	.3	4
NAV	1	4K IS, 4K DS	.2	3
	1[1]	4K IS, 4K DS	.2	3
	513		6.8	38
			120	1701

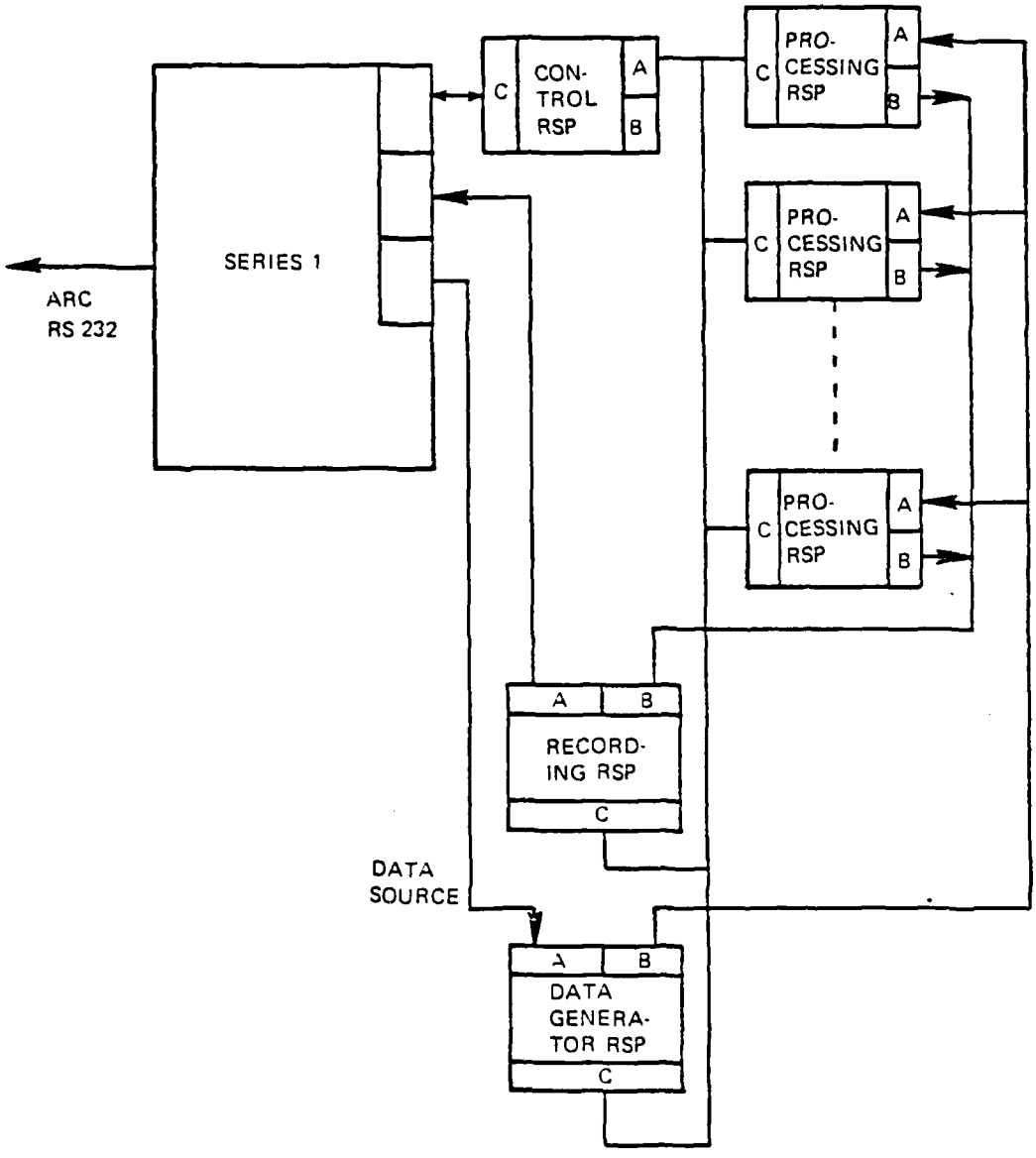
(1) Controllers

(2) IS - Instruction Store, DS - Data Store, BM - Bulk Memory

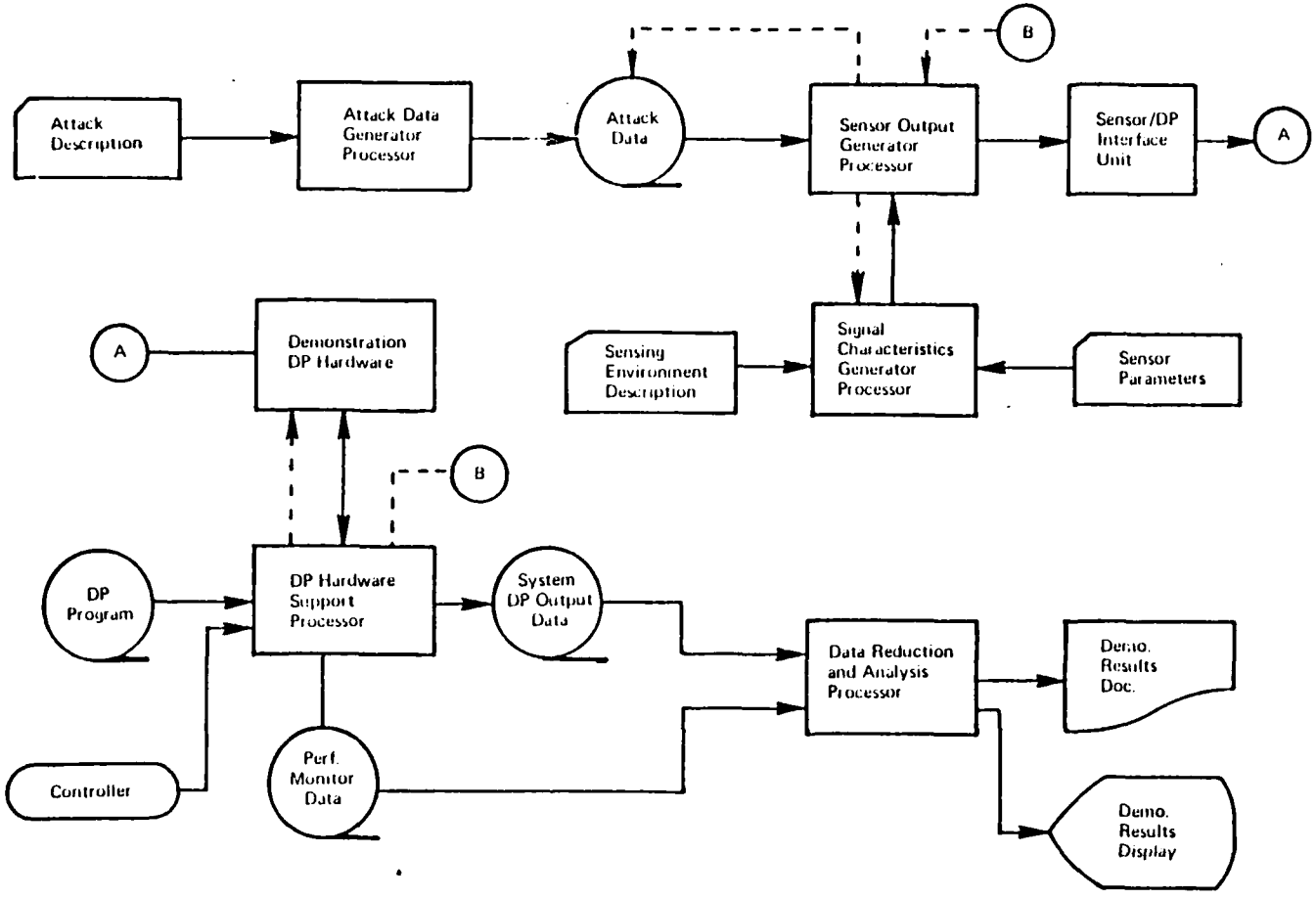
1990 Hardware Requirements for JSP Multifunction Implementation

Function	Processor Count	Memory[2] Per Processor (Words)
Input Signal	396 JSP	.8K IS, 2K DS, 12K BM
Conditioning	9 JSP[1]	.8K IS, 1K DS
Pulse Match,	9 JSP	1.6K IS, 4K DS, 12K BM
Superpoint	1 JSP[1]	.8K IS, 1K DS
Intraframe Correlation		
FEC	9 RSP	320K DS
CC	3 RSP	640K DS
SR, NC, DR	3 RSP	128K DS
	1 RSP[1]	16K DS
Interframe Correlation		
KOR	3 RSP	96K DS
FS	1 RSP	16K DS, 768K BM
TS	3 RSP	32K DS
AET	1 RSP	16K DS, 1723K BM
	1 RSP[1]	16K DS
Track and Discrimination		
PTD	16 RSP	10K IS, 16K DS, 384K BM
CP	1 RSP	16K DS
NAV	1 RSP	16K DS
	1 RSP	16K DS

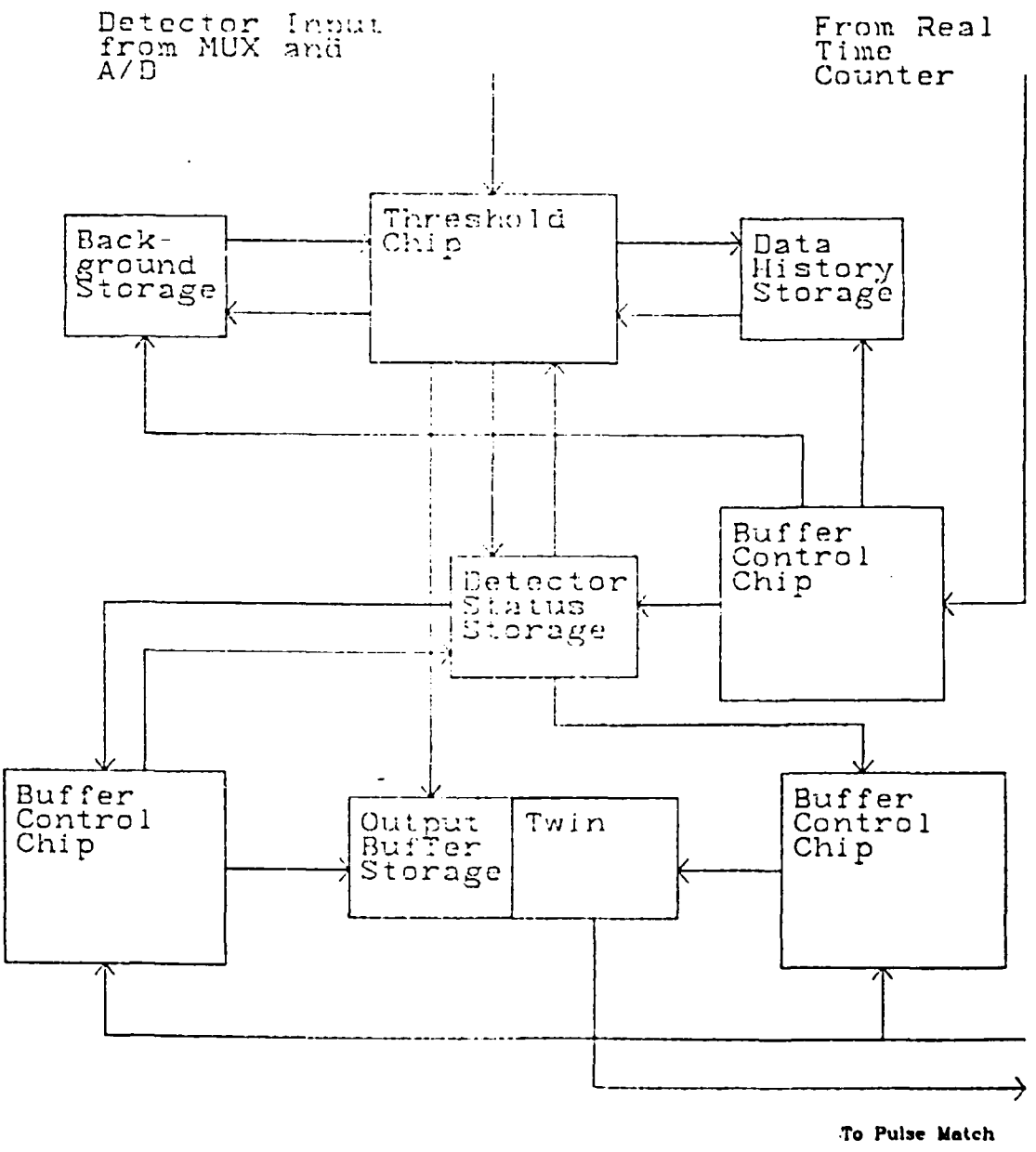
(1) Control Function
(2) IS = Instruction Store (Addition to Processor On-Chip), DS = Data Store, BM = Bulk Memory



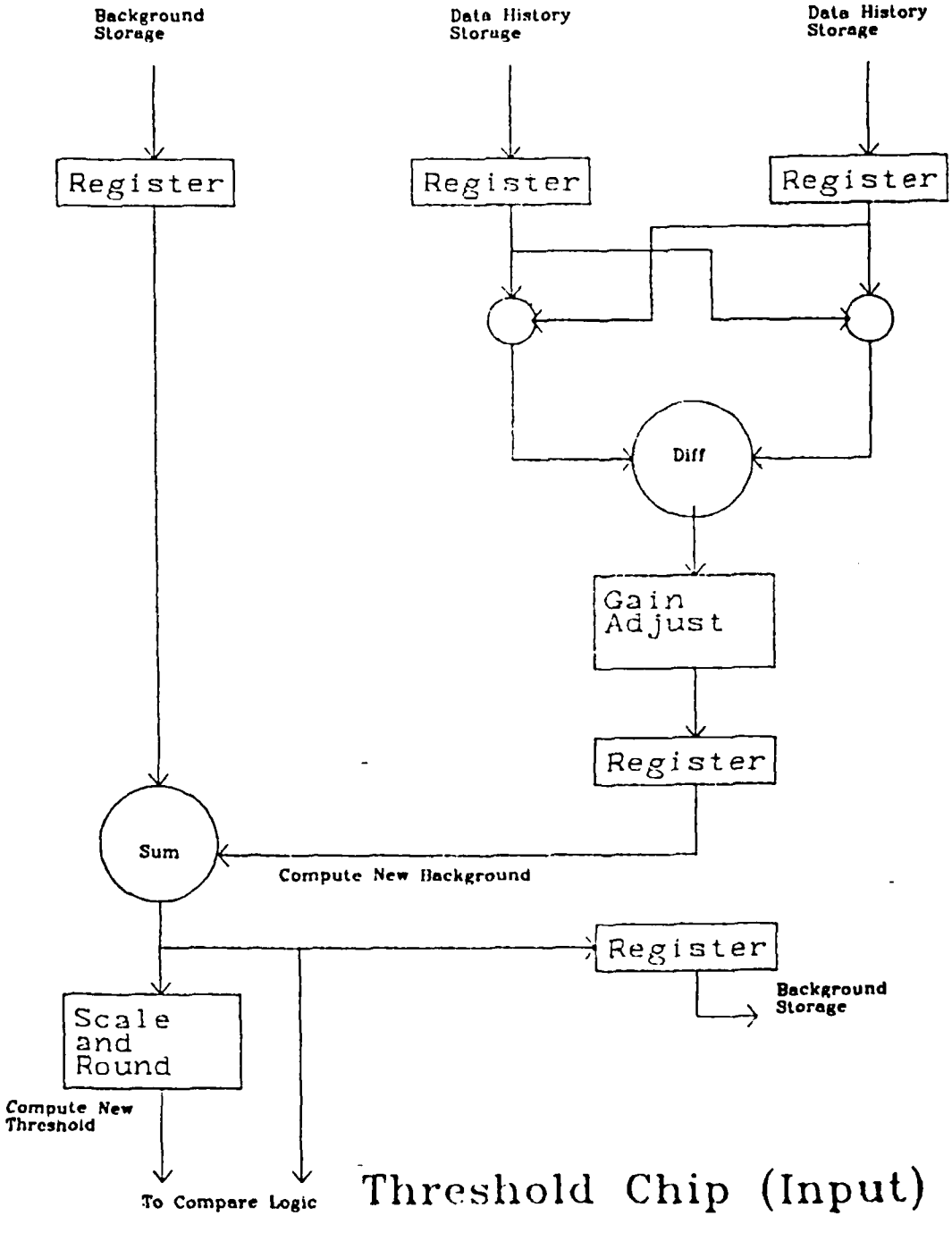
ARC Configuration for Input Recording Support



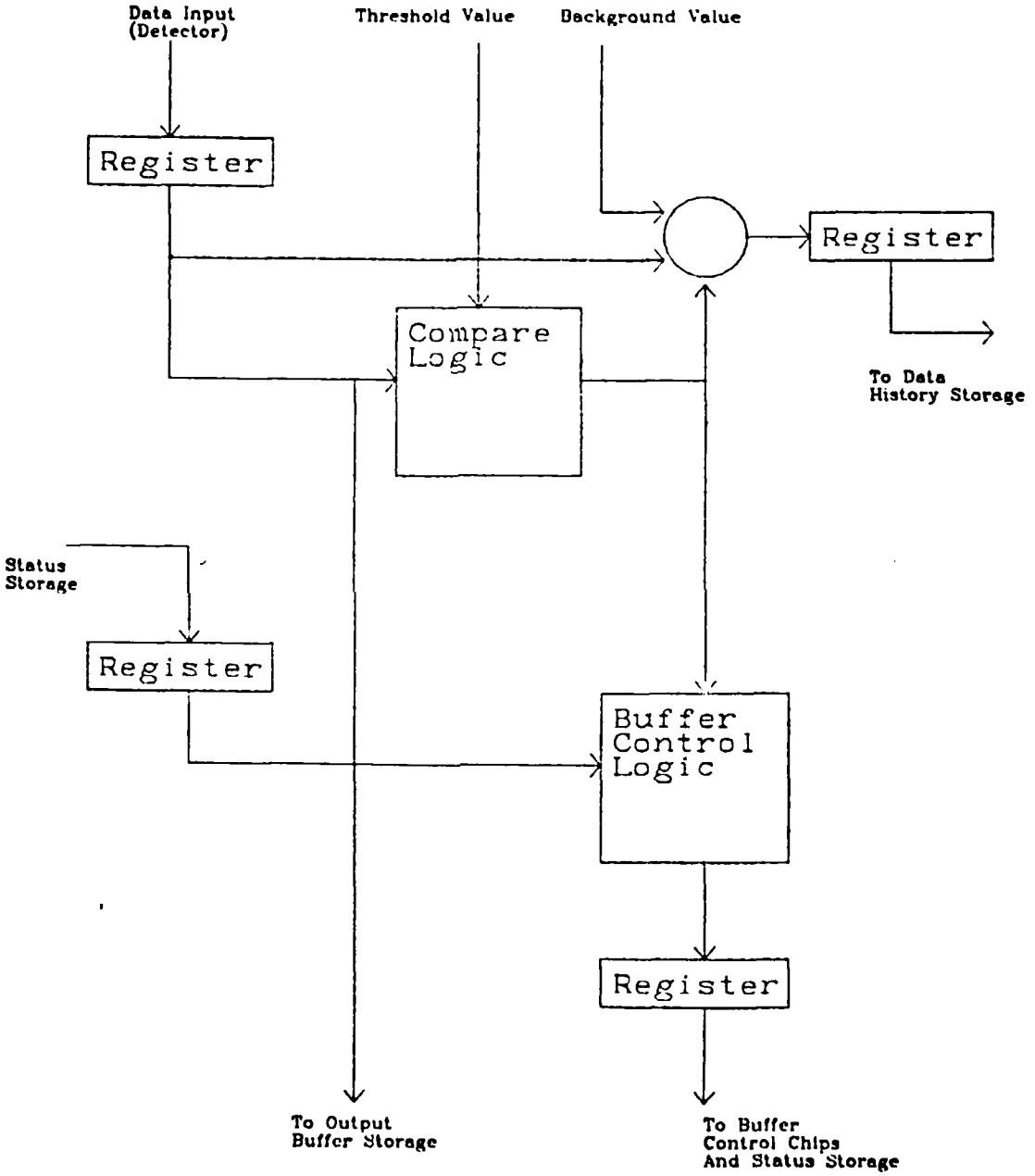
ARC Demonstration Configuration Requirement



ISC Overview



Threshold Chip (Input)



Threshold Chip (Output)

MSP SIZING

Type	*Quan*	*Pow*	*Sub-Tot*
ISC Threshold Chip	3	3w	12w
Buffer Control Chip	12	4w	48w
Memory 16k x 1 INMOS IMS-1400M	300	.7w	210w
Memory 4k x 4 INMOS IMS-1420M	250	.7w	175w
TTL Glue (MSI,SSI)	200	.1w	20w
Processor Chip	10	4w	40w
Total Power			505w

Board Count - 20
MSC Board (78 Dips, 9.0 in. x 6.27 in.)

END

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